A Thyristor based DC Fault Current Limiter with Inductor Inserting-Bypassing Capability

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***Abstract* — DC fault current limiters (FCL) are becoming increasingly important for the prompt DC fault clearance of modular multilevel converter (MMC) based HVDC grid. This paper proposes a hybrid FCL topology, in which the main current limiting circuit is composed of thyristors, capacitors and an inductor. Detailed theoretical analysis of the current limiting processes was carried out to check the electrical stresses. The relationship between the voltage stress and the current limiting time was analyzed, then a design method for the FCL parameters was provided. An effective method for fast bypassing the FCL inductor was proposed to reduce the energy dissipation when fault current is interrupted by a DC Circuit Breaker (DCCB). The dynamic performance of the proposed approach has shown that the proposed FCL can effectively limit the rate of rising of the DC fault current and reduce the energy dissipation.**

***Index Terms*—Modular multilevel converter (MMC); HVDC grid; fault current limiter (FCL); energy dissipation; DC Circuit Breaker (DCCB).**

NOMENCLATURE

DCCB	Direct current circuit breaker
FCL	Fault current limiter
LCS	Load commutation switch
UFD	Ultra fast disconnector
CFB	Current flow branch
IBB	Inductor bypassing branch
CCB	Current commutation branch
IB	Inductor branch
MOV	Metal-oxide varistor

I. INTRODUCTION

HIGH voltage direct current (HVDC) grids employing the modular multilevel converters (MMC) are considered to be one of the effective solutions for transferring the fluctuating renewable source energies over long distances through overhead transmission lines or cables [1]-[3]. A major challenge to the development of future HVDC grids is the countermeasures against DC-side short-circuit fault [4]. The DC line impedance is much smaller than ac line impedance, hence DC faults cause very large rate of rising of the fault currents. The hybrid DC circuit breaker (DCCB) can provide an effective solution to deal with DC faults [5]. However, high capital cost, large volume and weight are the main drawbacks of the current DCCBs [6]. Reduction of the interrupting current of DCCBs can contribute to reducing the total amount of energy dissipation in DCCBs, which in turn to decrease the size and weight of DCCBs.

For the purpose of reducing the interruption current, the intrinsic DC-side smoothing reactors are often installed at both ends of the DC transmission lines. However, the reactance cannot be too large, otherwise the construction cost will increase and the dynamic characteristics of the HVDC will be deteriorated [7]. Hence there is a need of DC fault current limiters (FCL) which are only activated when the DC fault current approaches a preset value without affecting the normal operation of HVDC grids.

FCLs can be classified into four categories:

- Superconducting FCLs [8], [9]. They utilize the zero-resistance characteristic and full diamagnetic resistance of the superconducting materials, which shows low impedance when the HVDC grid operates in normal state and turns into high impedance rapidly when a short-circuit fault occurs [8]. However, due to the high cost of the superconducting technology, it takes long time for them coming to real HVDC systems.
- Solid-state FCLs (SSFCL) [10], [11]. They use pure power electronic devices as switches, thus can operate within a very short period of time once the fault is detected. However, due to the limited voltage and current ratings of the individual device, the SSFCLs usually need hundreds of such devices, which brings large on-state losses and thus not widely employed in the HVDC systems. This drawback is very similar to the solid-state DCCBs [12], [13].
- Mechanical FCLs [14]. The FCLs use fast mechanical switch to break the normal current path at the zero-crossing of the AC currents and the current limiting impedance is connected to the short-circuit loop to limit the rate of rising of the fault current. In HVDC systems, similar to the mechanical DCCBs, the mechanical FCLs also need L-C resonance circuit to create a zero-crossing of the DC current. Although the world's first mechanical DCCB has been installed in a 160 kV HVDC link in China Southern Grid (CSG) [15], its applicability in higher DC voltage system such as 500 kV is not yet proved. Therefore, due to the technical challenge when creating the zero-crossing, the mechanical FCLs will encounter large difficulties in HVDC system.
- Hybrid FCLs. Unlike the hybrid DCCBs, there are very few references focusing on the hybrid FCLs. In [16] a hybrid DCCB with current limiting capability is proposed,

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which is essentially a reciprocating DCCB. In the case of a temporary DC fault, it can work as a fault current limiter without interrupting the DC fault currents. However, the current limiting mode of the DCCB in [16] can be only used in medium voltage range and not suitable for HVDC system. In [17], a hybrid DCCB uses fast thyristors to achieve the purpose of fault interruption is proposed. The DCCB structure takes full use of the thyristors and capacitors to transfer the fault currents between adjacent branches, therefore, minimized number of IGBTs are used and the overall cost as well as the power losses are significantly reduced.

Considering huge volume and weight of existing DCCBs for DC grids, a current limiting module within a hybrid DCCB [18,19] may lead to an unexpected increase of volume and weight, high complexity in operation, and difficulties in maintenance. It is easier to design a separate FCL to a DCCB for industrial installation. Due to the overcurrent demand for semi-conductors and energy dissipation demand of MOV are both related to current square, a reduction of fault current will significantly reduce the total investment. This is the main advantage and motivation to design the FCL. In addition, the two independent devices may benefit industrial manufacture and maintenance. Although one disadvantage of the FCL is the slight increase of the power losses under normal condition, this can be accepted as the total investment is reduced. The requirement on the coordination between FCL and DCCB could increase complexity, but this can be solved within system design and protection setting. Considering that the investment can be decreased by using FCL, it is worth of further studying the hybrid FCL under various fault and operation conditions.

This paper proposes a bidirectional hybrid FCL using fast thyristors and capacitors, compared to the Alstom Grid's hybrid DCCB structure proposed in [17], the technical features of the proposed FCL include:

- The proposed FCL will respond to a fault earlier than DCCB, thus the peak current of FCL will be less than using a DCCB only, and the voltage levels of these two devices are similar, ,so the required number of thyristors, capacitors, and surge arresters of the FCL are less than the DCCB in [17]
- When the companion DCCB of the proposed FCL is interrupting the fault current, the current limiting inductor in the proposed FCL is intentionally bypassed by the inductor bypass branch to accelerate the decay of the fault current, thus enabling faster operation of the DCCBs.
- The proposed FCL can naturally reduce the total energy dissipation in the companion DCCB, and the FCL inductor bypassing operation can further reduce the energies.

The rest of the paper is structured as follows: Section II presents the topology and basic current limiting process of the proposed FCL. Section Ⅲ carries out the detailed theoretical analysis of the current limiting process. Section IV shows how the FCL inductor is bypassed when DCCB interrupts the currents. Section V conducts the electromagnetic transient (EMT) simulations and Section VI concludes this paper.

II. Topology And Basic Principle Of The Proposed FCL

A. Topology of the Proposed FCL

Fig. 1 shows the proposed FCL, in order to limit the DC fault currents from both directions, all the devices are connected in parallel back-to-back, which are distinguished by subscripts "a" and "b". Note that in Fig. 1 single devices are drawn while in practice a lot of devices may need to be series connected to withstand the DC voltage.

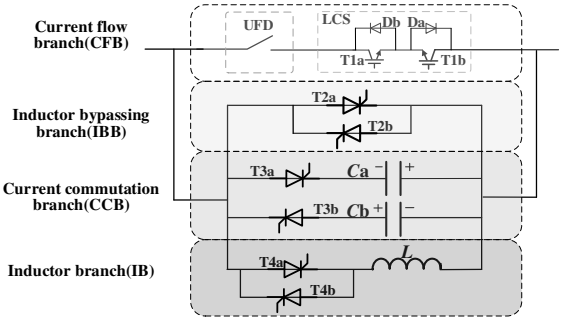

Fig. 1 The topology of the proposed FCL

The FCL has four branches, the detailed structure and function of these branches are introduced below:

- The current flow branch (CFB). It is composed of an ultrafast disconnector (UFD) and a load commutation switch (LCS), which is often used in the hybrid HVDC breakers [19]. The LCS is formed by IGBT valve T1 and diode valve D.
- The inductor bypassing branch (IBB). It is a thyristor valve T2, which is used for providing a bypassing path for the current , and can help to ensure reliable opening of the UFD at zero current and zero voltage.
- The current commutation branch (CCB). It includes the thyristor valve T3 and capacitor *C*. The capacitor is used to ensure the reliable turn-off of T2, and the reverse charging of the capacitor can store partial energies and suppress the rising rate of the fault current. Note that the capacitor voltage polarity in Fig.1 is the pre-charge direction of the capacitor and the capacitor has an on-line charging capability. Currently, the pre-charging of the capacitor in the HVDC system can use isolated auxiliary power supply or laser energy charger, and the initial voltage polarity of the capacitors are shown in Fig. 1.
- The inductor branch (IB). It is a series connection of the thyristor valve T4 and the current limiting inductor *L*. This branch is used to insert the FCL inductor *L* into the fault loop to suppress fault current rising. Ref. [17] uses a structure where the thyristor and capacitor are connected in series. It uses the clamping voltage of the arrester parallel with the capacitor to keep the voltage across the UFD sufficiently small when it is opening.

B. Current-Limiting Process Analysis

When the HVDC system is in normal operation, the UFD and LCS in the CFB shown in Fig. 1 are closed. Assume the FCL is located at the left side of the line, the fault current flowing through the FCL will be from left to right, then the current limiting process of the proposed FCL is as follows:

i. When the rate of rising and instantaneous value of the fault current value both exceed the preset threshold values, a turn-on signal is first sent to T2a, and the current will start to commutate to T2a immediately, then after a reasonable time delay (100μs in this paper), a turn-off signal is sent to LCS module. When the UFD current is smaller than the residual current, the UFD is signaled to open.

ii. After the UFD is fully open, a turn-on signal is sent to T3a and T4a, and T3a is turned on due to the forward-biased

voltage. Then *C*a starts to discharge and the voltage of *C*a is immediately imposed across T2a, which means the voltage on T2a is reverse biased. So the anode current of T2a will quickly drop to zero and the current in the FCL will be rapidly transferred from T2a branch to *C*a branch. When current in T2a is zero, *C*a is not fully discharged, T2a will continue to withstand reverse voltage provided by *C*a after a certain period of time and then turn off completely.

iii. After the voltage on *C*a drops to zero, *C*a continues to be charged in reverse, and T4a is turned on due to the forward-biased voltage, and then the current limiting inductor *L* is inserted into the fault circuit. At this moment, the fault current starts to charge the capacitor Ca, the increased Ca voltage can oppose the increase of the fault current. In addition, the Ca voltage make the T4a forward-biased and T4a is turned on as the pulse signal has already been sent to T4a. Thus L is also inserted into the circuit to limit the current.

The proposed FCL is an active device, and existing DC reactor is a passive device, which means the propose FCL provides a flexible choice in the change of inductance and make it easy to get a balance between system dynamic performance under steady state and current limiting performance under fault [20]. Superconducting FCL were proposed in [8,9], which however has more limitation in the overheating and less control flexibility comparing to the proposed thyristor based FCL. Existing variable magnetic inductors [21] can only be used in the low voltage level, while the thyristor based FCL can suit for various voltage levels. Comparing to other power electronics based FCL [22], the proposed thyristor based FCL uses capacitor discharge and recharge to insert additional inductor, which avoid the use of MOV and result in a soft current limiting process, which will bring benefit to extend the reliability of the power electronics devices.

III. Stage by Stage Theoretical Analysis of the Current Limiting Process

A. Theoretical Analysis

As shown in Fig. 2, assume the DC line is grounded at time t_0, where L_{dc} is a smoothing reactor, R_{line} and L_{line} are equivalent line impedances under lumped parameters. The cconverter station is modelled as a constant DC source U_{dc} and system inner resistance R_s. The results calculated with the DC source and the four-terminal bipolar HVDC grid simulation are shown in Section V. The reference directions for all the following physical variables are shown in Fig. 2. Note that the surge arresters for the semiconductor devices in the proposed FCL are not shown for simplicity purpose, and their configurations are similar to the hybrid DCCB reported in [17]. The symbols of all the timings during the fault current limiting process are given in Table 1.

Table 1 Symbols of the timing during the current limiting process

t_0	t_1	t_2	t_3	t_4	t_5
The fault occurs	Fault detected	The UFD is fully open	u_{Ca}=0 End of capacitor discharge	i_{Ca}=0 Inductor is fully inserted	DCCB starts to interrupt the current

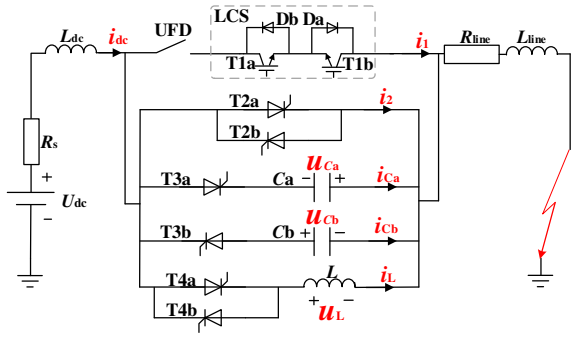

Fig. 2 Equivalent circuit of the FCL for analysis of the current limiting process.

Stage 1: $t_0 \le t \le t_2$

At t_0, the DC line current where the FCL is located rises. It is expressed as follows:

$$i_{dc} = \left(\frac{U_{dc}}{R_{line}+R_s} - I_n\right)\left(1 - e^{-\frac{t-t_0}{\tau_1}}\right) + I_n \tag{1}$$

Where, I_n is the rated current value of this line, and the time constant is given as:

$$\tau_1 = \frac{L_{dc} + L_{line}}{R_{line} + R_s} \tag{2}$$

After the overcurrent is detected at time t_1, the thyristor T2a is turned and the LCS is turned off after 100μs time delay. During $t_1 < t < t_2$, the current flows through T2a, the on-state resistances are sufficiently small that the DC current can still be expressed as (1).

Stage 2: $t_2 \le t \le t_3$

At t_2, the contacts of the UFD reach the rated open distance. At the same time, T3a receives the turn-on signal and it is turned on under forward-biased voltage. Due to the turn-on of T3a, the voltage of *C*a is imposed across T2a, and the voltage across T2a immediately becomes reversed and the anode current of T2a decreases rapidly. Since the initial voltage polarity of capacitor *C*a is opposite to the direction of the DC current, the DC current is rapidly drawn to the *C*a branch. Therefore, the fault current is rapidly transferred from T2a to T3a and *C*a, and this period of time can be ignored when conducting the theoretical analysis. Then the capacitor *C*a starts to discharge and the dynamic process can be described as:

$$\begin{cases} U_{dc} = (L_{dc} + L_{line})\dfrac{di_{Ca}}{dt} + (R_{line} + R_s)i_{Ca} - u_{Ca} \\ i_{Ca} = -C_a \dfrac{du_{Ca}}{dt} \end{cases} \tag{3}$$

The initial value of u_{ca} is U_0; ignoring the period of time when T2a current drops to zero, t_2 is substituted into (1) to obtain $i_{Ca}(t_2)=i_{DC}(t_2)=I_0$. By substituting the initial value into (3) we can obtain:

$$\begin{cases} u_{Ca} = \sqrt{D_1^2 + D_2^2}\, e^{\sigma(t-t_2)} \sin(\omega(t-t_2) + \varphi_1) - U_{dc} \\ i_{Ca} = C_a \sqrt{(\sigma^2 + \omega^2)(D_1^2 + D_2^2)}\, e^{\sigma(t-t_2)} \sin(\omega(t-t_2) + \varphi_2) \end{cases} \tag{4}$$

where, all the variables are defined as follows:

$$\begin{cases} \sigma = -\dfrac{R_{\text{line}} + R_{\text{s}}}{2(L_{\text{dc}} + L_{\text{line}})} \\ \omega = \sqrt{\dfrac{1}{C_{\text{a}}(L_{\text{dc}} + L_{\text{line}})} - \dfrac{(R_{\text{line}} + R_{\text{s}})^2}{4(L_{\text{dc}} + L_{\text{line}})^2}} \\ D_1 = U_0 + U_{\text{dc}} \\ D_2 = -\dfrac{I_0}{\text{C}_{\text{a}}\,\omega} - \dfrac{\sigma D_1}{\omega} \\ \tan\varphi_1 = \dfrac{D_1}{D_2}, \tan\varphi_2 = \dfrac{\sigma D_1 + \omega D_2}{\sigma D_2 - \omega D_1} \end{cases} \tag{5}$$

Although the anode current of the T2a decreases to zero rapidly, it still needs to withstand the reverse voltage for a certain period of time to make sure that its blocking capability is fully recovered. Therefore, to ensure that the discharge time of *C*a is not too short, the time duration that u_{ca} is greater than zero in (4) should be sufficiently long for T2a to be completely turned off. For this reason, special attentions should be paid on the design of the parameters, which will be discussed in next sub-section.

Stage 3: $t_3 \le t < t_4$

At t_3, u_{Ca}=0, *C*a just finished discharging, and then it begins to be charged in reverse. T4a is turned on due to the positive voltage. Ignoring the DC line resistance, system resistance and on-state voltage drop of thyristors T3a and T4a. Equation (6) can be obtained by KVL:

$$\begin{cases} U_{\text{dc}} = L_{\text{dc}}\dfrac{\text{d}i_{\text{dc}}}{\text{d}t} - u_{\text{Ca}} + L_{\text{line}}\dfrac{\text{d}i_{\text{dc}}}{\text{d}t} \\ U_{\text{dc}} = L_{\text{dc}}\dfrac{di_{\text{dc}}}{dt} + L\dfrac{\text{d}i_L}{\text{d}t} + L_{\text{line}}\dfrac{\text{d}i_{\text{dc}}}{\text{d}t} \\ i_{\text{Ca}} = -C_{\text{a}}\dfrac{\text{d}u_{\text{Ca}}}{\text{d}t} \\ i_{\text{Ca}} + i_L = i_{\text{dc}} \end{cases} \tag{6}$$

Equation (6) can be re-written as:

$$(L_{\text{dc}} + L_{\text{line}})C_{\text{a}}\frac{\text{d}^2u_{\text{Ca}}}{\text{d}t^2} + (\frac{L_{\text{dc}} + L_{\text{line}}}{L} + 1)u_{\text{Ca}} = -U_{\text{dc}} \tag{7}$$

The initial conditions are $u_{\text{Ca}}(t_3)$=0 and $i_{\text{Ca}}(t_3)=I_1$ obtained from (4) and (5). Substituting them into (7), yields

$$\begin{cases} u_{\text{Ca}} = \sqrt{E_1^{\,2} + E_2^{\,2}}\sin(\beta(t - t_3) + \alpha_1) - E_1 \\ i_{\text{Ca}} = \beta C_{\text{a}}\sqrt{E_1^{\,2} + E_2^{\,2}}\sin(\beta(t - t_3) + \alpha_2) \\ i_L = \dfrac{1}{\beta C_{\text{a}}}\sqrt{E_1^{\,2} + E_2^{\,2}}\sin(\beta(t - t_3) + \alpha_2) + \dfrac{E_1}{L}(t - t_3) - \dfrac{E_2}{\beta L} \end{cases} \tag{8}$$

where, all the variables are defined as follows:

$$\begin{cases} \beta = \sqrt{\dfrac{L_{\text{dc}} + L_{\text{line}} + L}{(L_{\text{dc}} + L_{\text{line}})LC_{\text{a}}}} \\ E_1 = \dfrac{U_{\text{dc}}L}{L_{\text{dc}} + L_{\text{line}} + L} \\ E_2 = -\dfrac{I_1}{C_{\text{a}}\beta} \\ \tan\alpha_1 = E_1 / E_2, \quad \tan\alpha_2 = -E_2 / E_1 \end{cases} \tag{9}$$

During the reverse charging process of *C*a, its voltage u_{Ca} will increase and its current i_{Ca} will decrease gradually. Although the system voltage is larger than the capacitor voltage, the difference is becoming smaller, and thus i_{dc} will keep raising but the rate of rising is decreasing accordingly. When the capacitor voltage is equal to the system voltage, the DC line current starts to decrease, and the voltages on the smoothing reactor and line inductance become negative. The capacitor voltage then gradually become higher than the system voltage. Assuming that i_{Ca} become zero at time t_4, then the voltage of *C*a rises to the maximum value $U_{\text{Ca\_max}}$ at this moment. This value affects the withstand voltage requirement for the thyristor valves T2 and T3.

Stage 4: $t_4 \le t \le t_5$

In order to get $U_{\text{Ca\_max}}$, t_4 should be calculated first. We can get multiple time values by setting i_{Ca} in (8) to be zero:

$$t = arctan\left(E_2 / E_1\right) / \beta + t_3 \tag{10}$$

Since tan*t* is a periodic function, multiple *t* can be obtained from (10), and t_4 is the smallest value which is greater than t_3. Then $U_{\text{Ca\_max}}=u_{\text{Ca}}(t_4)$ can be obtained by substituting t_4 into (8).

In the following we will check whether T3a can be turned off successfully, which is determined by the maximum positive voltage of T2a $U_{\text{T2a\_max}}$ and the maximum reverse voltage of T3a $U_{\text{T3a\_max}}$. At t_{4-}, the inductor voltage is equal to the voltage of *C*a; at t_4, the capacitor voltage reaches a maximum value, and the current i_{Ca} flows through T3a become zero; at t_{4+}, the capacitor branch CCB is disconnected. Ignoring the DC line resistance and system resistance, the voltage on T2a and T3a are easily obtained by KVL after t_4:

$$\begin{cases} u_{\text{T3a}}(t_{4+} \le t < t_5) = L\dfrac{\text{d}i_{\text{L}}}{\text{d}t} + U_{\text{Ca\_max}} \\ U_{\text{dc}} = L_{\text{dc}}\dfrac{\text{d}i_{\text{L}}}{\text{d}t} + L\dfrac{\text{d}i_{\text{L}}}{\text{d}t} + L_{\text{line}}\dfrac{\text{d}i_{\text{L}}}{\text{d}t} \\ u_{\text{T2a}}(t_{4+} \le t < t_5) = L\dfrac{\text{d}i_{\text{L}}}{\text{d}t} \end{cases} \tag{11}$$

Equation (11) can be further simplified as:

$$\begin{cases} u_{\text{T3a}}(t_{4+} \le t < t_5) = U_{\text{Ca\_max}} + \dfrac{U_{\text{dc}}L}{L_{\text{dc}} + L_{\text{line}} + L} \\ u_{\text{T2a}}(t_{4+} \le t < t_5) = \dfrac{U_{\text{dc}}L}{L_{\text{dc}} + L_{\text{line}} + L} \end{cases} \tag{12}$$

In (12), $U_{\text{Ca\_max}}$ is smaller than zero, and its absolute value is greater than U_{dc}. Therefore, the $u_{\text{T3a}(t4+)}$ must be smaller than

zero, and the thyristor valve T3a has to withstand reverse voltage immediately after t_4. Subsequently, T3a can be reliably turned off when the reverse voltage across it lasts for a certain period of time. Therefore, at t_4, u_{T3a} rises from zero to $u_{T3a}(t_{4+})$, and thus $U_{T3a\_max}=u_{T3a}(t_{4+})$; u_{T2a} changes from $-U_{ca\_max}$ to $u_{T2a}(t_{4+})$, and $U_{T2a\_max}=-U_{ca\_max}$.

After t_4, the DC fault current is completely commutated to the current limiting inductor branch (IB). Then $i_{dc}(t_4)=I_2$ is obtained by substituting t_4 into equations (6) and (8), then i_{dc} after t_4 is expressed as:

$$i_{dc}=(\frac{U_{dc}}{R_{line}+R_s}-I_2)(1-e^{-\frac{(t-t_2)}{\tau_2}})+I_2 \qquad (13)$$

where, time constant:

$$\tau_2=\frac{L_{dc}+L_{line}+L}{R_{line}+R_s} \qquad (14)$$

If the DCCBs do not operate, the DC current i_{dc} will increase according to (13). The insertion of the FCL inductor makes $\tau_2>\tau_1$, thus the rate of rising of the fault current will be noticeably decreased.

B. Parameter Design of the FCL

Based on the above analysis of the current limiting process, the design methods for the capacitance *C*a and the pre-charge voltage U_0 are discussed here.

The values of *C*a and U_0 have large impact on i) the voltage of the power electronic valve groups and ii) the operational timing sequence of the FCL. The valve groups include T1a, T2a, and T3a, where T1a withstands a small voltage because it is series connected with the UFD, and the voltages on T2a and T3a have been analyzed in detail in Section III. The maximum voltage across T4a is determined by the pre-charge voltage of Ca before it is turned on. The current limiter action time is (t_4-t_1), where (t_2-t_1) is the UFD action time, and (t_3-t_2) is the turn-off time of the thyristor T2, and both of them can be seen as constants. Therefore, only the charging duration of *C*a (t_4-t_3) is concerned here, which is represented by Δt_1.It is seen from equations (8) to (10) that the above two points i) and ii) are related to *C*a, *L*, and I_1.

For the FCL inductor *L*, its value can be initially determined according to the DC voltage level of the HVDC system and the requirements for the current limiting effect in the actual HVDC project. In this paper, a ±500 kV system is used, and *L* is selected to be 0.375H.

For I_1, $I_1=i_{Ca}(t_3)$ can be obtained from (4). It cannot be obtained in advance if *C*a is unknown, but it can be estimated. The reason is as follows: I_1 is the value of i_{Ca} when the capacitor voltage is zero. At this time, i_L is still zero, and thus I_1 is also equal to the current of the DC line i_{DC} (t_3); During t_2~t_3, *C*a discharges, and since *C*a is within microfarad range, the capacitor discharge has little impact on the fault current, thus I_1 is mainly determined by the HVDC system parameters. Since the discharge time of *C*a is very short, it can be estimated by $i_{dc}(t_2)$ in (1). In the ±500kV HVDC system, I_1 is calculated to be 15.46 kA by under the following preconditions, the smoothing reactance L_{dc} = 0.075H, I_n = 2 kA, R_{line} = 0, L_{line} = 0 (suppose the fault occurs at the end of the DC line), the opening time of the UFD is 2ms, and the preset threshold value for the DC fault is 1.2 I_n.

When *L* and I_1 are determined, the capacitance of *C*a can be designed. The relationship among *C*a, U_{T2a_max}, and Δt_1 can be obtained by substituting the above parameters into equations (8) to (10). And the relationship is shown in Fig 3.

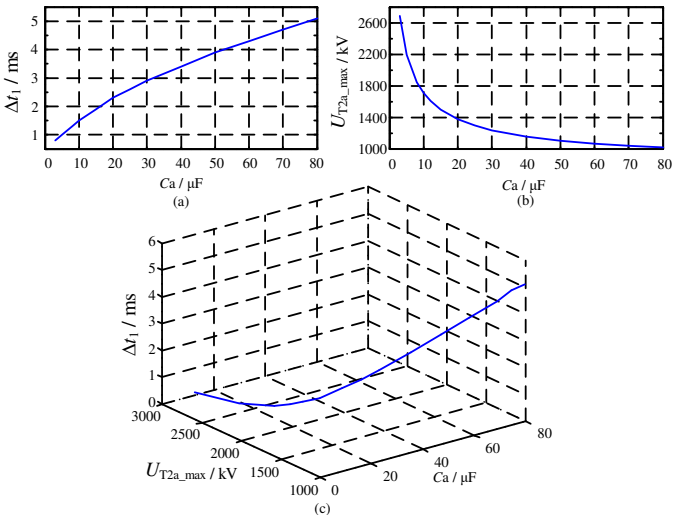

Fig. 3 Relationship of Ca, UT2a_max and Δt_1

In Fig. 3(a), the smaller *C*a corresponds to smaller Δt_1. This means as *C*a decreases, the required time for charging *C*a become shorter, and the FCL inductor can be inserted into the system faster. Further the DC current will drop faster due to *C*a's rapid charge. However, the smaller the *C*a is, the greater the maximum voltage across T2a will be, which is shown in Fig. 3(b). Especially starting from 10μF, as *C*a decreases, the maximum voltage of T2a increases rapidly. From 30μF, the maximum voltage of T2a changes slowly as *C*a increases. As shown in Fig. 3(c), when *C*a is between 10μF and 30μF, the maximum voltage of T2a is moderate and the current transfer time is relatively short. Therefore, it is recommended that the value of *C*a be selected between 10μF and 30μF.

From (12) it is seen that U_{T2a_max} and U_{T3a_max} only differ by a constant, hence only U_{T2a_max} is discussed here. After *C*a is determined, U_0 can be designed. To ensure that *C*a always provides reverse voltage to T2a during the turn-off process, U_0 can be obtained by setting the turn-off time to a given T_{off}, substituting $t=t_2+T_{off}$ into equations (4) and (5), and setting u_{Ca} in (4) to zero.This section aims to find feasible control objectives for the hybrid MMCs which can interrupt the source-side current feeding to the HVDC grid, and then propose suitable control strategies to achieve the control objectives.

IV. Fast Bypassing Of The Current Limiting Inductor

A. Fast Bypassing Process of the Inductor

The FCL is effective in decreasing the rate of rising of the fault currents, the companion DCCB which is responsible for interrupting the fault current in the faulted line will benefit from the FCL, in terms of either smaller interrupting current or longer allowed interruption time.

In the following, the hybrid DCCB topology [23] from ABB is selected to work as the companion DCCB of the proposed FCL for fault current interruption. After the action of the main circuit breaker, the arrester starts to dissipate energies,

and the fault current will descend immediately. However, the current limiting inductor in the fault circuit will decelerate the decay of the fault currents. In this paper, the FCL can use the thyristor valve T2 in the IBB to bypass the FCL inductor, thereby the proposed topology along with the control method can shorten the DCCB interruption time.

The overall process is described as follows:

i. Fault current commutation: When the overcurrent is detected, the proposed FCL and its companion DCCB start transferring the fault current at the same time: Both LCS modules are turned off, both UFDs begin to open, IGBTs in the DCCB main breaker are turned on, and T2a in the FCL is turned on, and the current path is shown in Fig.4 (a)

ii. Current limiting:. The fault current start to charge capacitor and current on the *L* raise gradually. The FCL starts to limit the fault current, as showed in Fig.4 (b).

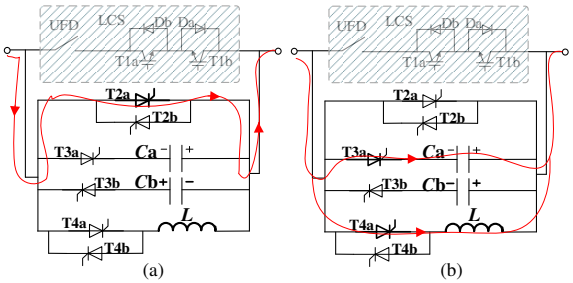

Fig. 4 Current flow diagram: (a) fault current commutation, (b) current limiting.

iii. Fast bypassing of the FCL inductor: When the protection system identifies the fault line, the DCCB receives the second triggering signal, the IGBTs in the DCCB main breaker are turned off, the arrester begins to consume energy, and the fault line current decreases rapidly. Then the voltage polarity of the inductor will become negative in Fig.2. Hence the voltage on T2b will be forward-biased and the T2b will be successfully turned on when the T2b is given a turn-on signal at the same time, and the current path is shown in Fig.5 (a). The inductor is then bypassed, since the current that flows through the inductor remains unchanged, the energies are temporarily stored there. The current in T2b is determined by the DC current and there is a circulation in *L* and T2b. Due to the arrester energy dissipation, the DC current continues to decrease. When fault current drops to zero, the disconnector in DCCB can completely clear the faulted line.

iv. Energy transfer of current limiting inductor: Because of the stored magnetic field energy of $1/2LI_3^2$ in the *L* and a circulation between *L* and T2b after the interruption, it is necessary to transfer this part of energy rapidly. Specifically, after the faulty line is isolated, a turn-on signal is sent to T3b. Then, similar to the current limiting principle described in Section I, the voltage on the capacitor *C*b first turns off T2b due to the reverse voltage, and then *C*b starts to be charged in reverse. The current path is shown in Fig. 5(b). The current in *L* gradually decreases to zero, and the energies stored in *L* are completely transferred to *C*b.

All the thyristors in the FCL will be selected according to the peak fault current across the FCL which occurs at the current limiting process. As analyzed in the subsection (iii) above for Fast bypassing of the FCL inductor, the fault current through the dc line was commutated to T2b gradually during the bypass process of the FCL, bypassing L doesn't cause any surge current. In addition, the current limit and fault current interruption take no more than 10ms, which is within the overcurrent tolerance capability a thyristor [24]. No overheat is expected. Thus the selection of the thyristor specifications according to the peak fault current is sufficient to ensure safe operation of the FCL.

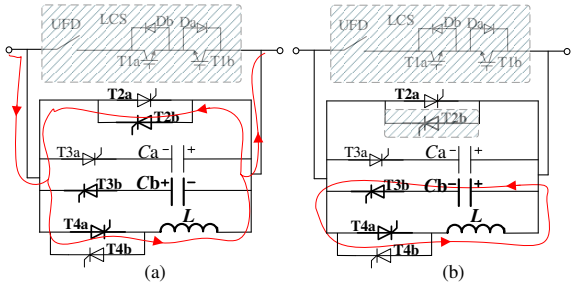

Fig. 5 Current flow diagram: (a) fast bypassing of inductor, (b) energy transfer of inductor.

B. Approximate Calculation of Reduced DCCB Energy Dissipation Due to the Inductor Bypassing

It is assumed that the IGBTs in the main breaker of the faulted line DCCB are turned off at t_5, then the arrester starts to consume energy, and the DC current drops to zero at t_6. The time period t_5~t_6 is recorded as the interruption time Δt_2. To calculate Δt_2, the energy dissipation of the arrester can be simplified by assuming that the arrester voltage is always held at its clamping voltage. The clamping voltage can be expressed as kU_{movn}, in which U_{movn} is the arrester rated voltage and k is a constant.

In Δt_2, ignoring the energy dissipation of the resistor, the energy conservation equation is as follows

$$\int_0^{\Delta t_2} U_{\mathrm{dc}} i_{\mathrm{dc}} \mathrm{d}t + \frac{1}{2} L_{\mathrm{e}} I_3^{\,2} = \int_0^{\Delta t_2} kU_{\mathrm{movn}} i_{\mathrm{dc}} \mathrm{d}t \tag{15}$$

where, L_{e} is the sum of the inductance in the fault circuit. The KVL equation of the circuit is given as:

$$L_{\mathrm{e}} \frac{\mathrm{d}i_{\mathrm{dc}}}{\mathrm{d}t} = -kU_{\mathrm{movn}} + U_{\mathrm{dc}} \tag{16}$$

I_3=$i_{\mathrm{dc}}(t_5)$ can be obtained from (13) by setting $t = t_5$. Then i_{dc} can be solved by substituting the initial value of I_3 into (16)

$$i_{\mathrm{dc}} = I_3 - \frac{kU_{\mathrm{movn}} - U_{\mathrm{dc}}}{L_{\mathrm{e}}} t \tag{17}$$

By substituting (17) into (15), after integration and simplification, the ultimate equation can be expressed as

$$-\frac{\gamma^2}{2L_{\mathrm{e}}} \Delta t^2 + \gamma I_3 \Delta t - \frac{1}{2} L_{\mathrm{e}} I_3^{\,2} = 0 \tag{18}$$

where, $\gamma = kU_{\mathrm{movn}} - U_{\mathrm{dc}}$.

The equation (18) can be solved as:

$$\Delta t_2 = L_{\mathrm{e}} I_3 / \gamma \tag{19}$$

When the arrester starts to consume energy, T2b is turned on and the FCL inductor is bypassed, then L_{e1}=L_{dc}+L_{line}. If no action is taken and the inductor still exists in the circuit, then

$L_{e2}=L_{dc}+L_{line}$. From (19), it can be seen that the reduction of L_e can reduce the interruption time Δt_2.

Referring back to equation (15), the reduction of Δt_2 causes the first term on the left side to decrease, which means the source side energy needs to be dissipated decreases. The reduction of L_e causes the second term on the left to decrease, which means the magnetic field energy is temporarily stored by L and does not need to be dissipated by the DCCB. By combing (15), (17), (19) and letting L_{e2} and L_{e1} to be L_e respectively, the reduced energy dissipation of the DCCB due to bypassing the FCL inductor can be obtained:

$$E_{save}=\frac{1}{2}LI_3^2\left(\frac{U_{dc}}{\gamma}+1\right) \tag{20}$$

where, U_{DC}/γ is a positive number, hence it can be seen that the reduced DCCB energy dissipation is considerable.

V. Model Validations

A. Theoretical Verification of FCL Operation Characteristics

The theoretical calculation and simulation results are compared in a single-ended equivalent system to verify the correctness of the theoretical analysis, the rationality of the parameter design, the current limiting effect, and the effect of bypassing the FCL inductor.

The schematic diagram of the simulation system is the same to Fig. 2. Rated DC voltage U_{dc}=±500kV, rated DC current I_n=2kA, equivalent internal resistance of the AC source Rs=1Ω, smoothing reactance L_{dc}=0.075H, R_{line}=0.5Ω, L_{line}=0.041H, the time for the UFD contacts to reach the rated open distance is 2ms, and the turnoff time for the fast thyristor is 50μs. According to the theoretical analysis, the designed capacitance Ca=Cb=15μF, the initial value of the capacitor voltage U_0=50kV, FCL inductance L=0.375H. The arrester rated voltage U_{movn}=500 kV, and k is taken as 1.96.

The single pole-to-ground fault shown in Fig. 2 is initiated at time t=0.3. The FCL and DCCB start current transfer when an overcurrent of 20% is detected, and all the switches and power electronics operate in the timing sequence described previously. The simulation results of the DC current, the CCB and IB current of the FCL, voltage across Ca, and the stress of each switching device in the current limiting and disconnecting processes are shown by the solid line in Fig. 6, the waveforms drawn from theoretical expressions are shown by the dotted line in Fig. 6.

In Fig. 6, the theoretical calculation and simulation waveforms match very well, which can prove the correctness of the theoretical analysis. The slight error in i_L and i_{dc} during t_3~t_4 is due to the fact that the small line resistance and system resistance are ignored in equation (6). However, if the resistance is taken into consideration, the analytical formulas will be more complicated. After t_4, the error of i_L is derived from the cumulative calculation error from t_3 to t_4, and the error of i_{dc} is derived from the difference between the simplified characteristics and the actual characteristics of arresters. For the enlarged part of time period t_2~t_3: Fig. 6(d) shows that u_{Ca} is reduced from 50kV to 0 during this period, which is the discharge process of Ca. Fig. 6(e) shows that u_{T2a} is always less than 0 during this period of time. The reverse voltage time on the thyristors is determined by capacitance, pre-charge voltage and fault current, in this simulation case, reverse voltage provided by the pre-charge capacitor is 65us and it is enough for thyristors reliable turning off. And this further proves the rationality of the parameter design methods of U_0 and Ca.

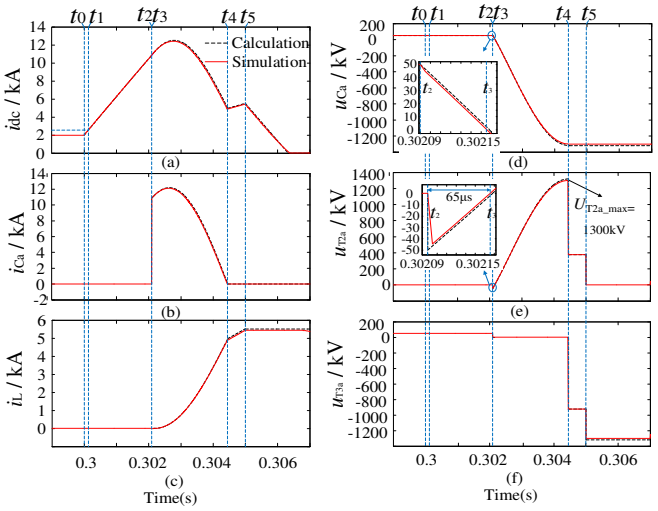

Fig. 6 Comparison of the calculation and simulation results: (a) the DC current, (b) the current of capacitor Ca, (c) the current of inductor L, (d) the voltage of capacitor Ca, (e) the voltage of capacitor T2a and (f) the voltage of capacitor T3a.

Focusing on the verification of the current limiting effect, when the DCCB is not operating, waveforms are plotted according to the expressions in section III.A and they are shown in Fig. 7 for two cases which are with the FCL and without the FCL.

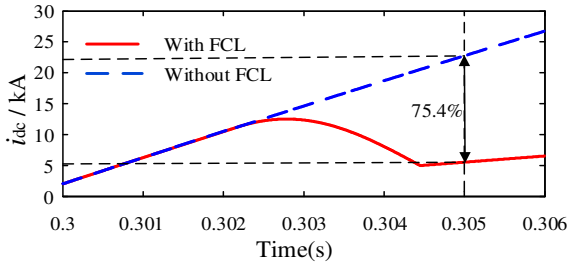

Fig. 7 Proposed FCL effect compared with free discharge fault current

It can be seen that the FCL reduces the DC fault current, the rate of rising of the fault current decreases after the FCL inductor is fully inserted, and the fault current at 5ms after the fault is reduced by 75.4%.

To verify the current limiting inductor bypassing effect, for two cases where inductor is bypassed or not in the DCCB interruption process. The comparison of DC current and energy dissipation in the DCCB is shown in Fig. 8.

The interruption time is shortened by 4.30ms in Fig. 8 (a). Substituting the parameters into equation (19), the interruption time Δt_2 is 1.33ms with the inductor bypassed, and Δt_2 is 5.64ms with the inductor remaining inserted, which is reduced by 4.31ms and is relatively close to 4.30ms. In Fig. 8 (b), the energy dissipated by the DCCB is reduced by 11.47MJ, which is pretty close to the energy E_{save} is 11.65MJ calculated from equation (20). The error mainly comes from assuming the surge arrester voltage remains unchanged.

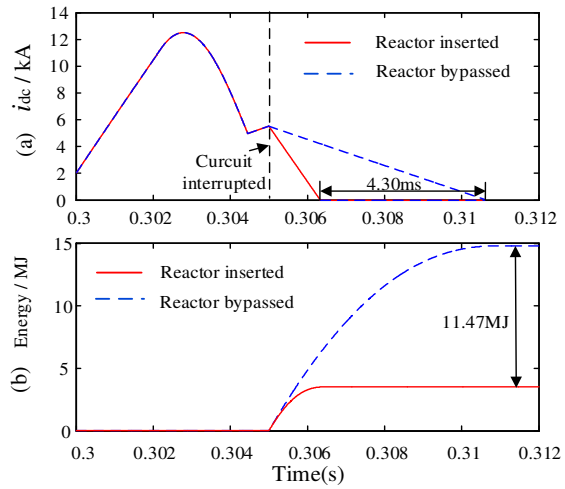

Fig. 8 Verification of the FCL inductor fast bypassing process.

In addition, in order to demonstrate the rationality of the inductor energy transfer process, the simulation results are shown in Fig. 9.

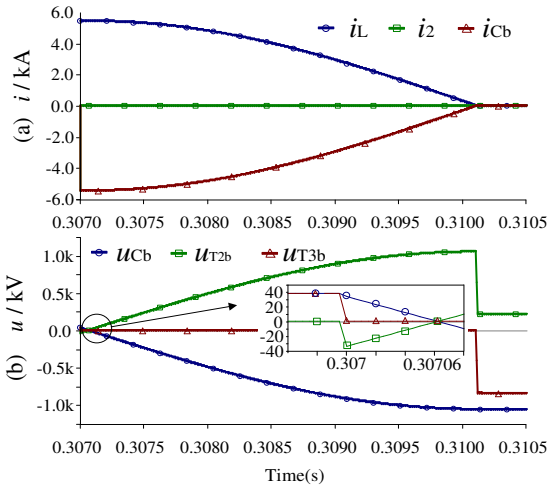

Fig. 9 Simulations of inductor energy transfer of FCL.

It can be seen from the enlarged part of Fig. 9 that T2b can withstand the reverse voltage of a period after the current has dropped to zero. As u_{Cb} gradually increases, i_L and i_{Cb} gradually drop to zero, and the energy in the inductor is completely transferred to the capacitor *C*b.

B. Verification in a Bipolar Four-terminal HVDC Grid

Fig. 10 is a schematic diagram of a ±500kV four-terminal HVDC grid. The converter station has a bipolar structure. The overhead lines adopt the frequency-dependent model in PSCAD. The rated DC current between the MMC1 and MMC4 station is 2 kA, and the FCL parameters are the same as in Section V. A. At t=1s, a positive pole-to-ground fault occurs at the midpoint point of the Line 14.

When a fault is detected, the FCL is triggered using a lower threshold value, and It takes longer time for the DCCB to operate due to a higher threshold and discriminative relaying protection. When a DCCB senses an occurrence of a fault, it takes more time to judge if the fault is within the protection zone of the DCCB before operating the DCCB. Thus, it is not possible to operate a DCCB earlier. However a FCL can operate immediately after sensing the occurrence of a fault without considering selectivity. The fault current is limited to a much smaller value when the DCCB start to operate, thus only a small capacity of DCCB is needed. Although the operation of the FCL could affect fault current profile which in turn influences the fault detection and discrimination of the DCCB, proper protection settings can be designed to avoid inaccurate operation of the DCCB. When the FCL is triggered by a short disturbance, and DCCB is triggered by protection system. The FCL will be restored to normal operation by reclosing its current flow branch. The energy storage in the inductor can be absorbed through energy transfer process in Section IV.

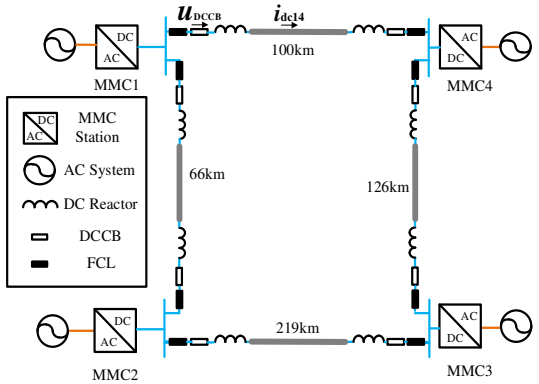

Fig. 10 Diagram of four-terminal bipolar HVDC grid.

Fig. 11 shows the simulation results of all the branch currents when the FCL and DCCB at the DC bus of MMC1 operate and the current limiting inductor is bypassed during the DCCB interruption. The overall trend is the same as in Section V. A. The main reason for the difference in value and current ripple is that the R-L lumped parameters used in the theoretical analysis may not accurately reproduce the frequency characteristics of the actual transmission line [25], [26]. Another reason is the discharge and coupling of the capacitances of the converter sub-modules in the HVDC grid.

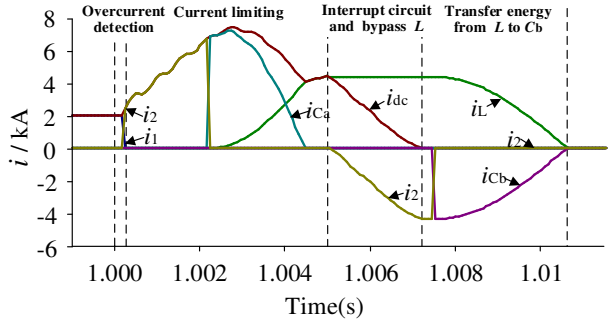

Fig. 11 Simulation waveforms of FCL applied in HVDC grid.

In order to verify current limiting and inductor bypassing effects of the proposed FCL, three scenarios are compared, in the first scenario, the FCL does not act, only the DCCB operates; And in the second scenario, FCL acts, but the current limiting inductor is not bypassed during the DCCB interruption. In the third scenario, FCL acts and bypassed when the DCCB interruption. Respectively shows the comparison of the DC fault current, DCCB voltage, and DCCB energy dissipation in the above three cases.

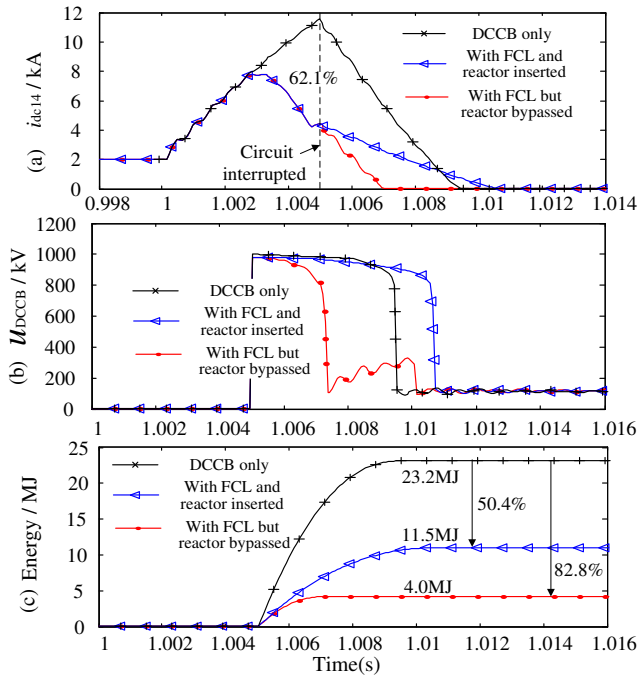

Fig. 12 Comparison of three cases: (a) DC current (b) voltage on DCCB (c) energy dissipation in MOV

Fig.12 (a) shows that, due to the current limiting the fault current is reduced by 62.1% within 5ms after the fault. The bypassing of current limiting inductor accelerates the interruption process of the DCCBs. If the FCL inductor is not bypassed, although the fault current is reduced, the larger inductor will prevent fault current decrease, and the interruption time will increase. Fig. 11(b) shows that the peak voltages of DCCBs are almost identical, this is due to the overvoltage of DCCB is mainly determined by the threshold DC voltage value of the MOV, which is the same in all three cases. In the case when the FCL inductor is bypassed, the interruption time is the shortest and the voltage drop process is the fastest.

It can be seen from Fig. 12(c) that, although the interruption time is slightly increased in the case when the inductor is not bypassed, the energy dissipation is still reduced because the fault current is significantly reduced. Since the current limiting and bypassing of the inductor reduce the interruption time and the fault current, the total energy dissipation is reduced by 82.8%, which reduces the requirements for the DCCB arrester to a large extent.

VI. Conclusions

This paper proposes a hybrid fault current limiter (FCL) and investigates its operating principle, parameter design, and the FCL inductor bypassing during interruption of DCCBs.

The the thyristors to be help turned off through the pre-charged capacitor, and the current limiting inductor can be inserted with simple logic. Capacitor charging and the insertion of the FCL inductor can effectively suppress the rising of the fault current. The FCL and its control logics are applied on a four-terminal bipolar MMC-HVDC grid. After 5ms of the fault, the fault line current is reduced by 62.1%.

During the process of DCCB interruption, the FCL inductor is intentionally bypassed, which can shorten the interruption time, and further reduce the total amount of energies to be dissipated in the DCCBs. The energy dissipation is reduced by 82.8% in this paper.

References

[1] T. An, X Zhou, C Han Y Wu, Z He, H Pang and G Tang, “A DC grid benchmark model for studies of interconnection of power systems,” *CSEE Journal of Power and Energy Systems*, vol.1, no.4, pp.101-109, Dec. 2015.

[2] T. An, G. Tang, and W. Wang, “Research and application on multi-terminal and DC grids based on VSC-HVDC technology in China,” *IET High Voltage* vol.2, no.1, pp.1-10, 2017.

[3] Juan Manuel Carrasco et al., “Power-Electronic System for the Grid Integration of Renewable Energy Sources: A Survey,” *IEEE Trans. Industrial Electronics*, vol. 53, no.4, pp. 1002-1016, Aug. 2006.

[4] G. Liu, F. Xu, Z. Xu, Z. Zhang, and G. Tang, “Assembly HVDC breaker for HVDC grids with modular multilevel converters,” *IEEE Trans. Power Electron*., vol. 32, no. 2, pp. 931–941, Feb. 2017.

[5] R.Derakhshanfar at all, “Hybrid HVDC breaker – A solution for future HVDC system” CIGRE paris 2014, B4-304.

[6] Wang Wenyuan, Barnes M, Marjanovic O, et al., “Impact of DC breaker systems on multiterminal VSC-HVDC stability,” *IEEE Trans. Power Del*., vol. 31, no. 2, pp. 769-779, April. 2016.

[7] Beerten J， D'Arco S， Suul J A． “Identification and small-signal analysis of interaction modes in VSC MTDC systems,” *IEEE Trans. Power Del*., vol. 31, no. 2, pp. 888-897, April. 2016.

[8] M. Jangale and K. D. Thakur. “Optimum positioning of superconducting fault current limiter for wind farm fault current in smart grid.[C]//2017 International conference of Electronics,” *Communication and Aerospace Technology* vol.2, pp. 312-316, 2017.

[9] U. A. Khan, J. G. Lee, F. Amir and B. W. Lee, "A Novel Model of HVDC Hybrid-Type Superconducting Circuit Breaker and Its Performance Analysis for Limiting and Breaking DC Fault Currents," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 6, pp. 1-9, Dec. 2015.

[10] A. R. Fereidouni, B. Vahidi and T. Hosseini Mehr, "The Impact of Solid State Fault Current Limiter on Power Network With Wind-Turbine Power Generation," *IEEE Trans. Smart Grid*, vol. 4, no. 2, pp. 1188-1196, June 2013.

[11] H. Radmanesh, S. H. Fathi, G. B. Gharehpetian, et al . "Bridge-Type Solid-State Fault Current Limiter Based on AC/DC Reactor," in IEEE Transactions on Power Delivery, vol. 31, no. 1, pp. 200-209, Feb. 2016.

[12] Kapoor R, Shukla A, Demetriades G. “State of art of power electronics in circuit breaker technology,” *Energy Conversion Congress and Exposition. IEEE*, pp.615-622,2012.

[13] Jianguo M, Li W, Jie H. “Research on main circuit topology for a novel DC solid-state circuit breaker,” *IEEE Conference on Industrial Electronics and Applications*, pp.926-930, 2010.

[14] W. Lin, D. Jovcic, S. Nguefeu and H. Saad, “Modelling of High Power Mechanical DC Circuit breaker,” APPEEC, Brisbane, November 2015.

[15] CHEN Ming, XU Hui, ZHANG Zu’an, LI Xiaolin, RAO Hong, YUAN Zhao. Design and Simulation of Coupling Mechanical High Voltage DC Circuit Breaker. High Voltage Engineering. Vol.44, No.2: 380-387(in Chinese).

[16] D. Keshavarzi, E. Farjah and T. Ghanbari, "Hybrid DC Circuit Breaker and Fault Current Limiter With Optional Interruption Capability," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2330-2338, March 2018.

[17] Aliakbar Jamshidi Far and Dragan Jovcic, “Design, Modeling and Control of Hybrid DC Circuit Breaker Based on Fast Thyristors,” *IEEE Trans. Power Del*., vol. 33, no. 2, pp. 919–927, April. 2018.

[18] B. Li, J. He, Y. Li and R. Li, "A Novel Solid-state Circuit Breaker with Self-adapt Fault Current Limiting Capability for LVDC Distribution Network," in *IEEE Transactions on Power Electronics*. (early access).

[19] K. Yang et al., "Direct-Current Vacuum Circuit Breaker With Superconducting Fault-Current Limiter," in *IEEE Trans on Appl Superconductivity*, vol. 28, no. 1, pp. 1-8, Jan. 2018.

[20] M. S. Alam, A. Hussein, M. A. Abido and Z. M. Al-Hamouz, "VSC-HVDC system stability augmentation with bridge type fault current limiter, *2017 6th International Conference on Clean Electrical Power (ICCEP)*, Santa Margherita Ligure, 2017, pp. 531-535

[21] J. M. Alonso, G. Martínez, M. Perdigão, M. R. Cosetin and R. N. do Prado, "A Systematic Approach to Modeling Complex Magnetic Devices Using SPICE: Application to Variable Inductors," in IEEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7735-7746, Nov. 2016.

[22] A. R. Fereidouni, B. Vahidi and T. Hosseini Mehr, "The Impact of Solid State Fault Current Limiter on Power Network With Wind-Turbine Power Generation," in IEEE Transactions on Smart Grid, vol. 4, no. 2, pp. 1188-1196, June 2013.
[23] A. Hassanpoor, J. Häfner and B. Jacobson, "Technical Assessment of Load Commutation Switch in Hybrid HVDC Breaker," *IEEE Trans. Power Electron.*, vol.30, no.10, pp.5393-5400, Oct. 2015.
[24] "5STP 45Y8500 data sheet", ABB Semiconductor, Lenzburg, Switzerland, 2017 Oct 16. http://www.abb.com.
[25] Noda T. "Application of frequency-partitioning fitting to the phase-domain frequency-dependent modeling of overhead transmission lines," *IEEE Trans. Power Del*., vol. 30, no. 1, pp. 174–183, July. 2014.
[26] Noda T, Nagaoka N, Ametani A. "Phase domain modeling of frequency-dependent transmission lines by means of an ARMA model," *IEEE Trans. Power Del*., vol. 11, no. 1, pp. 401-411, Jan 1996.

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